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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,491	01/07/2004	Keith W. Jones	AFD 602	5435

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EXAMINER	
MONIKANG, GEORGE C	

ART UNIT	PAPER NUMBER
2615	

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06/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,491	JONES ET AL.	
	Examiner	Art Unit	
	GEORGE C. MONIKANG	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/7/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroyanagi et al, US Patent 4,782,246, in view of Herring, US Patent Pub. 2002/0001317 A1.

Re Claim 1, Kuroyanagi et al disclose an inexpensive and programmable amplitude and phase shifting circuit comprising: an enclosure comprising: a plurality of signal sending digital control lines routed to an amplitude/phase shifting circuit board; and means for selecting a single amplifier for operator selected amplitude or phase gain change (*Kuroyanagi et al, abstract; , col. 4, lines 34-42*); an amplitude/phase shifting circuit board comprising: a plurality of

programmable gain operational amplifiers (*Kuroyanagi et al, col. 4, lines 34-42*), one amplifier selected at a time to have its gain changed when an operator desires a new amplitude or phase (*Kuroyanagi et al, abstract; col. 4, lines 34-42*); each of said digital control lines connected to a different multiplying operational amplifier chip select line on said amplitude/phase shifting circuit board (*Kuroyanagi et al, col. 4, lines 34-42*); and means for controlling said amplitude/phase shifting circuit (*Kuroyanagi et al, col. 4, lines 34-42*); but fails to disclose means for holding printing circuit boards and a front panel for receiving input and output signals (*Herring, fig. 3*); a motherboard comprising: means for supplying input signals through said front panel (*Herring, fig. 3*); a power source (*Herring, fig. 3: power button of cell phone*); digital control lines; and a demultiplexer circuit board (*Herring, para 0053*); said demultiplexer circuit board within said motherboard comprising: a plurality of signal receiving digital control lines from a digital output card in a personal computer (*Herring, fig. 3; para 0053*); and a plurality of signal receiving digital control lines for receiving output lines from said demultiplexer (*Herring, fig. 3; para 0053*). However, Herring does.

Taking the combined teachings of Kuroyanagi et al and Herring as a whole, one skilled in the art would have found it obvious to modify the inexpensive and programmable amplitude and phase shifting circuit comprising: an enclosure comprising: a plurality of signal sending digital control lines routed to an amplitude/phase shifting circuit board; and means for selecting a single amplifier for operator selected amplitude or phase gain change (*Kuroyanagi et al, abstract; col. 4, lines 34-42*); an amplitude/phase shifting circuit board

comprising: a plurality of programmable gain operational amplifiers (*Kuroyanagi et al, col. 4, lines 34-42*), one amplifier selected at a time to have its gain changed when an operator desires a new amplitude or phase (*Kuroyanagi et al, abstract; col. 4, lines 34-42*); each of said digital control lines connected to a different multiplying operational amplifier chip select line on said amplitude/phase shifting circuit board (*Kuroyanagi et al, col. 4, lines 34-42*); and means for controlling said amplitude/phase shifting circuit (*Kuroyanagi et al, col. 4, lines 34-42*) with disclose means for holding printing circuit boards and a front panel for receiving input and output signals (*Herring, fig. 3*); a motherboard comprising: means for supplying input signals through said front panel (*Herring, fig. 3*); a power source (*Herring, fig. 3: power button of cell phone*); digital control lines; and a demultiplexer circuit board (*Herring, para 0053*); said demultiplexer circuit board within said motherboard comprising: a plurality of signal receiving digital control lines from a digital output card in a personal computer (*Herring, fig. 3; para 0053*); and a plurality of signal receiving digital control lines for receiving output lines from said demultiplexer (*Herring, fig. 3; para 0053*) in order to be able to detect the phase difference between input and output signals within a computer device

Re Claim 2, which further recites, “Wherein said enclosure further comprises a front panel for receiving sine and cosine input signals and phase shifted output signals.” Kuroyanagi et al and Herring fail to disclose sine and cosine signals being generated as claimed. Official notice is taken that both the concepts and advantages of generating sine and cosine signals are well known

in the art. Thus it would have been obvious to use sine and cosine signals since sine and cosine are merely functions of signals.

Re Claim 3, the combined teachings of Kuroyanagi et al and Herring disclose the amplitude and phase shifting circuit of claim 1 wherein said enclosure mounts onto a standard electronics rack (*Herring, fig. 3: cell phone of Herring can be mounted in a cell phone holder*).

Re Claim 4, which further recites, "Wherein said demultiplexer further comprises a 50-pin ribbon cable connector for accepting digital control lines coming from digital output card in a personal computer." Kuroyanagi et al and Herring fail to disclose a 50-pin ribbon cable as claimed. Official notice is taken that both the concepts and advantages of providing a 50-pin ribbon cable are well known in the art. Thus it would have been obvious to use a 50-pin ribbon cable since they are commonly used as input output adapters.

Re Claim 5, the combined teachings of Kuroyanagi et al and Herring disclose the amplitude and phase shifting circuit of claim 1 wherein said means for controlling said amplitude/phase shifting circuit comprises a digital output card from a personal computer (*Herring, fig. 3: cell phone comprises a card*).

Claim 6 has been analyzed and rejected according to claim 4.

Re Claim 7, the combined teachings of Kuroyanagi et al and Herring disclose the amplitude and phase shifting circuit of claim 5 wherein an operator

interfaces with said digital output card through software (*Herring, fig. 3: cell phone comprises a card*).

Re Claim 8, which further recites, "Wherein an operator interfaces with said digital output card through LabVIEW ™ software." Kuroyanagi et al and Herring fail to disclose the use of LabVIEW to output the digital signals. Official notice is taken that both the concepts and advantages of using LabVIEW to output Digital signals are well known in the art. Thus it would have been obvious to use LabVIEW since it is commonly used for data acquisition.

Claim 9 has been analyzed and rejected according to claim 1. Claim 9 also further discloses the phase shifting circuit having a plurality of channels. The combined teachings of Kuroyanagi et al and Herring disclose a phase shifting circuit implemented multiple channel cell phone (*Herring, para 0004*).

Claims 10 & 15 have been analyzed and rejected according to claims 2 & 9.

Claims 11 & 12 have been analyzed and rejected according to claims 5 & 9.

Claim 13 has been analyzed and rejected according to claims 8-9.

Claim 14 has been analyzed and rejected according to claims 4 & 9.

Re Claim 16, the combined teachings of Kuroyanagi et al and Herring disclose the inexpensive, programmable, multiple channel amplitude and phase

shifting method of claim 9 wherein said selecting step further comprises the steps of: determining timing and sequence of reading data lines from said motherboard (*Herring, para 0053*); storing data in a buffer (*Herring, fig. 3: cell phone comprises storage means*); and changing gain of a selected operational amplifie (*Kuroyanagi et al, col. 4, lines 34-42*).

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEORGE C. MONIKANG whose telephone number is (571)270-1190. The examiner can normally be reached on M-F. alt Fri. Off 7:30am-5:00pm (est).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chin Vivian can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/George C Monikang/ 6/20/2008
Examiner, Art Unit 2615

/Vivian Chin/
Supervisory Patent Examiner, Art Unit 2615

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